PATENT ABSTRACTS OF JAPAN

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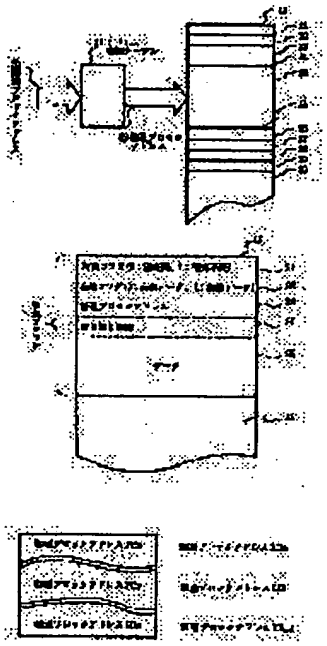
(54) NON-VOLATILE SEMICONDUCTOR MEMORY AND ITS CONTROL METHOD

(57)Abstract:
PURPOSE: To perform rewriting operation at high speed by providing a table which converts a logic block address to a physical block address at the time of reading and writing operation of a block.
CONSTITUTION: A table 31 stored at a position indicated with a logical block address LBi of an address conversion table 31 is read out, and a physical block address PBi corresponding to the LBi is obtained. Next, an erasing flag in the PBi is written and set to zero requiring for erasing. Next, a erasing flag and a valid flag of the physical block in a nonvolatile semiconductor memory are successively read out, and a physical block PBk in which the both are '1' is obtained. Next, new data of the LBi is written in a data section in the PBk, a valid flag is set to zero indicating validity, and the LBi is written in a logical block address section 32. Further, the content PBi stored at a position indicated with the LBi of the table 31 is rewritten to the PBk. Thereby, when the LBi is accessed thereafter, the PBk is read out from the table 31.



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ABSTRACTED-PUB-NO: JP 07153284A

BASIC-ABSTRACT:

The non-volatile semiconductor memory is organised into multiple blocks. An erasing flag, on effective flag and a logical block address are stored for every block. When re-writing the data of the logical block, the physical block which corresponds to this is not erased immediately. An erasing flag is written in the relevant field. Then, the data is written in the physical block.

An effective flag is written in the relevant field. The physical block is erased during the period in which the data access is not performed. A conversion table is used to obtain the physical address from the logical address during the above referred read/write operations.

ADVANTAGE - Hides slow erasing process. Reduces number of re-write times.

CHOSEN-DRAWING: Dwg.1/4

TITLE-TERMS: NON VOLATILE SEMICONDUCTOR MEMORY EEPROM CONVERT TABLE CONVERT LOGIC ADDRESS PHYSICAL ADDRESS READ WRITING OPERATE CANDIDATE BLOCK BLOCK ERASE NON ACCESS PERIOD

DERWENT-CLASS: U13 U14

EPI-CODES: U13-C04B2; U14-A08;

TECHNICAL FIELD

[Industrial Application] This invention relates to the control approach of non-volatile semiconductor memories, such as read-only memory (EEPROM) in which rewriting and elimination are possible, electrically especially about the control approach of a non-volatile semiconductor memory.

EFFECT OF THE INVENTION

[Effect of the Invention] Thus, according to this invention, when rewriting the data of a logical block, the physical block corresponding to a logical block is not eliminated promptly, but it asks for the physical block which is not written [both an elimination flag and whose an effective flag are "1"] in, and data are written in at the block, and since a block is eliminated at the period which has not been accessed, elimination actuation [low speed / in activation] can be concealed. Moreover, since the physical block to write in changes for every rewriting even if rewriting concentrates on the same logical block, rewriting is not completed to a specific physical block, but the count of rewriting decreases. Furthermore, since the address translation table changed into a physical block address from a logic block address is not made to fix to a specific storage area but the logical address is made to memorize for every physical block, the correction writing of the address translation table accompanying actuation does not concentrate on rewriting at a specific storage area. For this reason, the count of rewriting decreases and high reliance-ization can be realized.

PRIOR ART

[Description of the Prior Art] Conventionally, since this kind of non-volatile semiconductor memory has low rewritable counts as about 10,000 times, the control approach of the non-volatile semiconductor memory for improving this has already been released to many reference, such as JP,63-181190,A.
[0003] For example, the control approach given [above-mentioned] in JP,63-181190,A (reference 1) reduces the count of rewriting for every block by dividing the memory area of a non-volatile semiconductor memory into two or more blocks, and changing the block for sequential writing for every rewriting.
[0004] Moreover, a memory area is divided into two or more blocks like reference 1, the rewriting improper flag set for every block when it is the rewriting improper block which is not rewritable is prepared, when the block for rewriting is a rewriting improper block, the above-mentioned improper flag is set and data are made for the control approach

given in JP,4-57298,A (reference 2) to write in to other blocks.
[0005] Furthermore, the control approach given in JP,1-286199,A (reference 3) is a thing of making the count of rewriting increase by replacing a write-in bad block with other intact blocks using random access memory (RAM) with EEPROM which divided the memory area into two or more blocks like reference 1.
[0006] However, in this way, when a power source is shut off at the period when the above-mentioned write data is stored only in RAM, as for the approach of storing a write data in RAM temporarily, the above-mentioned write data will be destroyed.
[0007] Moreover, the block number which the software which uses a non-volatile semiconductor memory (memory) manages when changing a write-in block in any [of reference 1-3] case, About the translation table for matching with a response, i.e., a logical-block number, and a physical block number with the physical block number of the above-mentioned memory Since no cure to the approach of volatilize[un-]-izing or the reduction approach of the count of a store also has explanation and the concrete approach of ****** is not realized Rewriting of the above-mentioned translation table is needed for every modification of a block, and the count of rewriting of the above-mentioned translation table which consists of the above-mentioned memory is not reduced, but becomes the inhibition factor of a raise in reliance.
[0008] Furthermore, since elimination actuation [low speed originally] follows on the rewriting actuation in the case of changing a write-in block, this kind of the control approach is a low speed intrinsically.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] The approach the control approach of the conventional non-volatile semiconductor memory mentioned above stores a write data in RAM temporarily had the fault that the non-volatile of storage information could not necessarily secure.
[0010] Moreover, since the translation table for matching with the logical-block number in the case of changing a write-in block and a physical block number needed to be rewritten, there was a fault that the count of a store was irreducible.
[0011] Furthermore, since elimination actuation [low speed originally] followed on the rewriting actuation in the case of changing a write-in block, there was a fault that this rewriting actuation served as a low speed intrinsically.

MEANS

[Means for Solving the Problem] The non-volatile semiconductor memory of this invention The count of rewriting of the elimination flag field which consists of the sector of two or more memory capacity defined beforehand, and stores an elimination flag for every physical block of said block at least, the effective flag field which stores an effective flag, the logic block-address field which stores a logic block address, and said physical block It consists of two or more blocks which have the count field of rewriting to store, and the data area which stores data. In the non-volatile semiconductor memory which performs each elimination of the content of storing of said elimination flag, said effective flag, said logic block address, and said count of rewriting in the unit of said

block, and performs read-out write-in actuation of said block of each in the unit of said sector It is the configuration equipped with the translation table changed into a physical block address from said logic block address at the time of read-out write-in actuation of said block.

[0013] Moreover, the control approach of the non-volatile semiconductor memory of this invention The count of rewriting of the elimination flag field which consists of the sector of two or more memory capacity defined beforehand, and stores an elimination flag for every physical block of said block at least, the effective flag field which stores an effective flag, the logic block-address field which stores a logic block address, and said physical block It consists of two or more blocks which have the count field of rewriting to store, and the data area which stores data. In the control approach of a non-volatile semiconductor memory of performing each elimination of the content of storing of said elimination flag, said effective flag, said logic block address, and said count of rewriting in the unit of said block, and performing read-out write-in actuation of said block of each in the unit of said sector It has the translation table changed into a physical block address from said logic block address at the time of read-out write-in actuation of said block. In case data are rewritten, the data specified by said logic block address It asks for the 1st physical block address corresponding to said logic block address from said address translation table. The elimination flag field of the 1st block specified by this 1st physical block address is written in important point elimination. It asks for the 2nd physical block address [finishing / elimination] an elimination flag indicates elimination needlessness to be and an effective flag indicates an invalid to be. The effective flag which is specified by this 2nd physical block address and which shows validity is written in the effective flag field of a block of said logic block address of the write-in above 2nd to the logic block-address field of a block of said data of the write-in above 2nd in the data area of the 2nd block. Said 2nd physical block address is written in the address specified by said logic block address of said address translation table. An elimination flag is important point elimination at the period when it is made to correspond to the storage condition after eliminating the invalid of the elimination needlessness of the elimination flag of said 1st block, and the effective flag of said 1st block at, and said non-volatile semiconductor memory is not accessed. An effective flag an invalid It is characterized by eliminating the shown block.

[0014] Furthermore, the control approach of the non-volatile semiconductor memory of this invention is characterized by rewriting at the period when said non-volatile semiconductor memory is not accessed, and eliminating little block of a count.

EXAMPLE

[Example] Next, the example of this invention is explained with reference to a drawing.

[0016] Drawing 2 is the block diagram showing each block of the non-volatile semiconductor memory of one example of this invention.

[0017] The non-volatile semiconductor memory of this example assumes the crash memory chip of the memory capacity of 4M bit, i.e., a 512K cutting tool, on **** of explanation. This memory chip consists of 32 blocks whose block sizes are 16 K bytes, and each block consists of 31 sectors with a sector size of 512 bytes.

[0018] When drawing 2 is reference, the physical block 10 of the nonvolatile storage of this example consists of the elimination flag field 21, the effective flag field 22, a logic block-address field 23, a count field 24 of rewriting, and a data area 25. Moreover, the nonvolatile storage of this example is the configuration of having two or more physical blocks equivalent to the above-mentioned physical block 10, and having the address translation table 31 which changes the logic block address 32 into the physical block address 33 further.

[0019] Drawing 3 (A) is drawing explaining a format of the physical block of the nonvolatile storage of this example, and drawing 3 (B) is drawing explaining a format of the address translation table of this example.

[0020] By the control approach of the non-volatilized student semiconductor memory shown in this example, elimination is performed in the block unit shown in drawing 3 (A). It is shown whether an elimination flag should eliminate a block and logical-value"0" shows important point elimination. It is shown whether an effective flag has effective data of a block, and logical-value"0" shows validity. Content"of storage1" is in the storage condition of not writing in. Therefore, the storage condition after the block was eliminated becomes logical-value"1" altogether including a flag, an elimination flag shows elimination needlessness and an effective flag shows an invalid data, respectively.

[0021] The block which is going to access this non-volatile semiconductor memory is first specified by the logic block address. The physical block address PBi corresponding to the location where the address translation table shown in drawing 3 (B) is shown by the logic block address LBi is memorized. The reading output of the address translation table of the location shown by the logic block address LBi serves as the physical block address PBi. Content setting out of this address translation table is all performed after powering on by writing in the physical block address corresponding to the address translation table of the location specified by the logic block address of this non-volatile semiconductor memory which read the logic block address of a block and was read.

[0022] Next, the control approach of the non-volatile semiconductor memory of the 1st example of this invention is explained. Drawing 1 is a flow chart which shows the 1st example of this invention.

[0023] If it explains simultaneously with reference to drawing 3 (A), drawing 1 (B), and drawing 1 , the control approach of this example will be performed by the procedure of step S1 to the step S6.

[0024] That is, the address translation table of the location shown by the logic block address LBi of an address translation table is read at step S1, and it asks for the physical block address PBi corresponding to the logic block address LBi. At step S2, the elimination flag in a physical block PBi is written in, and it sets to "0" which shows important point elimination. At step S3, the elimination flag and effective flag of a physical block in this non-volatile semiconductor memory are read one by one, and both an elimination flag and an effective flag ask for the physical block PBk of "1." By step S4, it sets to "0" which writes the new data of a logical block LBi in the data division in a physical block PBk, writes in an effective flag, and shows validity by things, and LBi is written in the logic block-address section.

[0025] Furthermore, the content PBi of the location shown by the logic block address LBi of an address translation table at step S5 is rewritten to PBk. Thereby, when accessing a logical block LBi henceforth, reading appearance of the physical block PBk is carried out

from an address translation table. At step S6, elimination actuation of the physical block by which the elimination flag is set to "0" which shows important point elimination at the period when the non-volatilized student semiconductor memory is not accessed is performed. If access is made during elimination actuation, elimination actuation is interrupted, priority will be given to the access and it will be performed.
[0026] Reading actuation of a logical block LBi is easily made by beginning to compose the data of the block specified by the physical block address PBi for which read the content of the address translation table of the location specified by the logic block address, and asked for the physical block address PBi, and the degree was asked as the above explanation.
[0027] Next, the control approach of the non-volatile semiconductor memory of the 2nd example of this invention is explained.
[0028] If drawing 4 is referred to, since step S1 to the step S6 of the control approach of this example is the same as that of the control approach of the 1st example, it stops to illustrate to the flow chart of drawing 4 , and detailed explanation is omitted.
[0029] Next, after step S6 is completed, at step S7, the count of rewriting eliminates few physical blocks at the period when this non-volatile semiconductor memory is not accessed.
[0030] By this, the control which does not concentrate rewriting on a specific physical block can carry out more easily.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is a flow chart explaining the control approach of the nonvolatile storage of the 1st example of this invention.
[Drawing 2] It is the block diagram of a block of the nonvolatile storage of one example of this invention.
[Drawing 3] They are a format (A) of a block of one example of this invention, and the explanatory view of an address translation table (B).
[Drawing 4] It is a flow chart explaining the control approach of the nonvolatile storage of the 2nd example of this invention.
[Description of Notations]
10 11 Physical block
21 26 Elimination flag field
22 27 Effective flag field
23 28 Logical address field
24 29 Count field of rewriting
25 30 Data area
31 Address Translation Table
32 Logic Block Address
33 Physical Block Address
S1-S7 Control step

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the control approach of non-volatile semiconductor memories, such as read-only memory (EEPROM) in which rewriting and elimination are possible, electrically especially about the control approach of a non-volatile semiconductor memory.
[0002]
[Description of the Prior Art] Conventionally, since this kind of non-volatile semiconductor memory has low rewritable counts as about 10,000 times, the control approach of the non-volatile semiconductor memory for improving this has already been released to many reference, such as JP,63-181190,A.
[0003] For example, the control approach given [above-mentioned] in JP,63-181190,A (reference 1) reduces the count of rewriting for every block by dividing the memory area of a non-volatile semiconductor memory into two or more blocks, and changing the block for sequential writing for every rewriting.
[0004] Moreover, a memory area is divided into two or more blocks like reference 1, the rewriting improper flag set for every block when it is the rewriting improper block which is not rewritable is prepared, when the block for rewriting is a rewriting improper block, the above-mentioned improper flag is set and data are made for the control approach given in JP,4-57298,A (reference 2) to write in to other blocks.
[0005] Furthermore, the control approach given in JP,1-286199,A (reference 3) is a thing of making the count of rewriting increase by replacing a write-in bad block with other intact blocks using random access memory (RAM) with EEPROM which divided the memory area into two or more blocks like reference 1.
[0006] However, in this way, when a power source is shut off at the period when the above-mentioned write data is stored only in RAM, as for the approach of storing a write data in RAM temporarily, the above-mentioned write data will be destroyed.
[0007] Moreover, the block number which the software which uses a non-volatile semiconductor memory (memory) manages when changing a write-in block in any [of reference 1-3] case, About the translation table for matching with a response, i.e., a logical-block number, and a physical block number with the physical block number of the above-mentioned memory Since no cure to the approach of volatilize[un-]-izing or the reduction approach of the count of a store also has explanation and the concrete approach of ****** is not realized Rewriting of the above-mentioned translation table is needed for every modification of a block, and the count of rewriting of the above-mentioned translation table which consists of the above-mentioned memory is not reduced, but becomes the inhibition factor of a raise in reliance.
[0008] Furthermore, since elimination actuation [low speed originally] follows on the rewriting actuation in the case of changing a write-in block, this kind of the control approach is a low speed intrinsically.
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[0012]
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[0013] Moreover, the control approach of the non-volatile semiconductor memory of this invention The count of rewriting of the elimination flag field which consists of the sector of two or more memory capacity defined beforehand, and stores an elimination flag for every physical block of said block at least, the effective flag field which stores an effective flag, the logic block-address field which stores a logic block address, and said physical block It consists of two or more blocks which have the count field of rewriting to store, and the data area which stores data. In the control approach of a non-volatile semiconductor memory of performing each elimination of the content of storing of said elimination flag, said effective flag, said logic block address, and said count of rewriting in the unit of said block, and performing read-out write-in actuation of said block of each in the unit of said sector It has the translation table changed into a physical block address from said logic block address at the time of read-out write-in actuation of said block. In case data are rewritten, the data specified by said logic block address It asks for the 1st physical block address corresponding to said logic block address from said address translation table. The elimination flag field of the 1st block specified by this 1st physical block address is written in important point elimination. It asks for the 2nd physical block address [finishing / elimination] an elimination flag indicates elimination needlessness to be and an effective flag indicates an invalid to be. The effective flag which is specified by this 2nd physical block address and which shows validity is written in the effective flag field of a block of said logic block address of the write-in above 2nd to the logic block-address field of a block of said data of the write-in above 2nd in the data area of the 2nd block. Said 2nd physical block address is written in the address specified by said logic block address of said address translation table. An elimination flag is important point elimination at the period when it is made to correspond to the storage condition after eliminating the invalid of the elimination needlessness of the elimination flag of said 1st block, and the effective flag of said 1st block at, and said non-volatile semiconductor

memory is not accessed. An effective flag an invalid It is characterized by eliminating the shown block.
[0014] Furthermore, the control approach of the non-volatile semiconductor memory of this invention is characterized by rewriting at the period when said non-volatile semiconductor memory is not accessed, and eliminating little block of a count.
[0015]
[Example] Next, the example of this invention is explained with reference to a drawing.
[0016] Drawing 2 is the block diagram showing each block of the non-volatile semiconductor memory of one example of this invention.
[0017] The non-volatile semiconductor memory of this example assumes the crash memory chip of the memory capacity of 4M bit, i.e., a 512K cutting tool, on **** of explanation. This memory chip consists of 32 blocks whose block sizes are 16 K bytes, and each block consists of 31 sectors with a sector size of 512 bytes.
[0018] When drawing 2 is reference, the physical block 10 of the nonvolatile storage of this example consists of the elimination flag field 21, the effective flag field 22, a logic block-address field 23, a count field 24 of rewriting, and a data area 25. Moreover, the nonvolatile storage of this example is the configuration of having two or more physical blocks equivalent to the above-mentioned physical block 10, and having the address translation table 31 which changes the logic block address 32 into the physical block address 33 further.
[0019] Drawing 3 (A) is drawing explaining a format of the physical block of the nonvolatile storage of this example, and drawing 3 (B) is drawing explaining a format of the address translation table of this example.
[0020] By the control approach of the non-volatilized student semiconductor memory shown in this example, elimination is performed in the block unit shown in drawing 3 (A). It is shown whether an elimination flag should eliminate a block and logical-value"0" shows important point elimination. It is shown whether an effective flag has effective data of a block, and logical-value"0" shows validity. Content"of storage1" is in the storage condition of not writing in. Therefore, the storage condition after the block was eliminated becomes logical-value"1" altogether including a flag, an elimination flag shows elimination needlessness and an effective flag shows an invalid data, respectively.
[0021] The block which is going to access this non-volatile semiconductor memory is first specified by the logic block address. The physical block address PBi corresponding to the location where the address translation table shown in drawing 3 (B) is shown by the logic block address LBi is memorized. The reading output of the address translation table of the location shown by the logic block address LBi serves as the physical block address PBi. Content setting out of this address translation table is all performed after powering on by writing in the physical block address corresponding to the address translation table of the location specified by the logic block address of this non-volatile semiconductor memory which read the logic block address of a block and was read.
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[0025] Furthermore, the content PBi of the location shown by the logic block address LBi of an address translation table at step S5 is rewritten to PBk. Thereby, when accessing a logical block LBi henceforth, reading appearance of the physical block PBk is carried out from an address translation table. At step S6, elimination actuation of the physical block by which the elimination flag is set to "0" which shows important point elimination at the period when the non-volatilized student semiconductor memory is not accessed is performed. If access is made during elimination actuation, elimination actuation is interrupted, priority will be given to the access and it will be performed.
[0026] Reading actuation of a logical block LBi is easily made by beginning to compose the data of the block specified by the physical block address PBi for which read the content of the address translation table of the location specified by the logic block address, and asked for the physical block address PBi, and the degree was asked as the above explanation.
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[0029] Next, after step S6 is completed, at step S7, the count of rewriting eliminates few physical blocks at the period when this non-volatile semiconductor memory is not accessed.
[0030] By this, the control which does not concentrate rewriting on a specific physical block can carry out more easily.
[0031]
[Effect of the Invention] Thus, according to this invention, when rewriting the data of a logical block, the physical block corresponding to a logical block is not eliminated promptly, but it asks for the physical block which is not written [both an elimination flag and whose an effective flag are "1"] in, and data are written in at the block, and since a block is eliminated at the period which has not been accessed, elimination actuation [low speed / in activation] can be concealed. Moreover, since the physical block to write in changes for every rewriting even if rewriting concentrates on the same logical block, rewriting is not completed to a specific physical block, but the count of rewriting decreases. Furthermore, since the address translation table changed into a physical block address from a logic block address is not made to fix to a specific storage area but the logical address is made to memorize for every physical block, the correction writing of the address translation table accompanying actuation does not concentrate on rewriting at

a specific storage area. For this reason, the count of rewriting decreases and high reliance-ization can be realized.

CLAIMS

[Claim(s)]

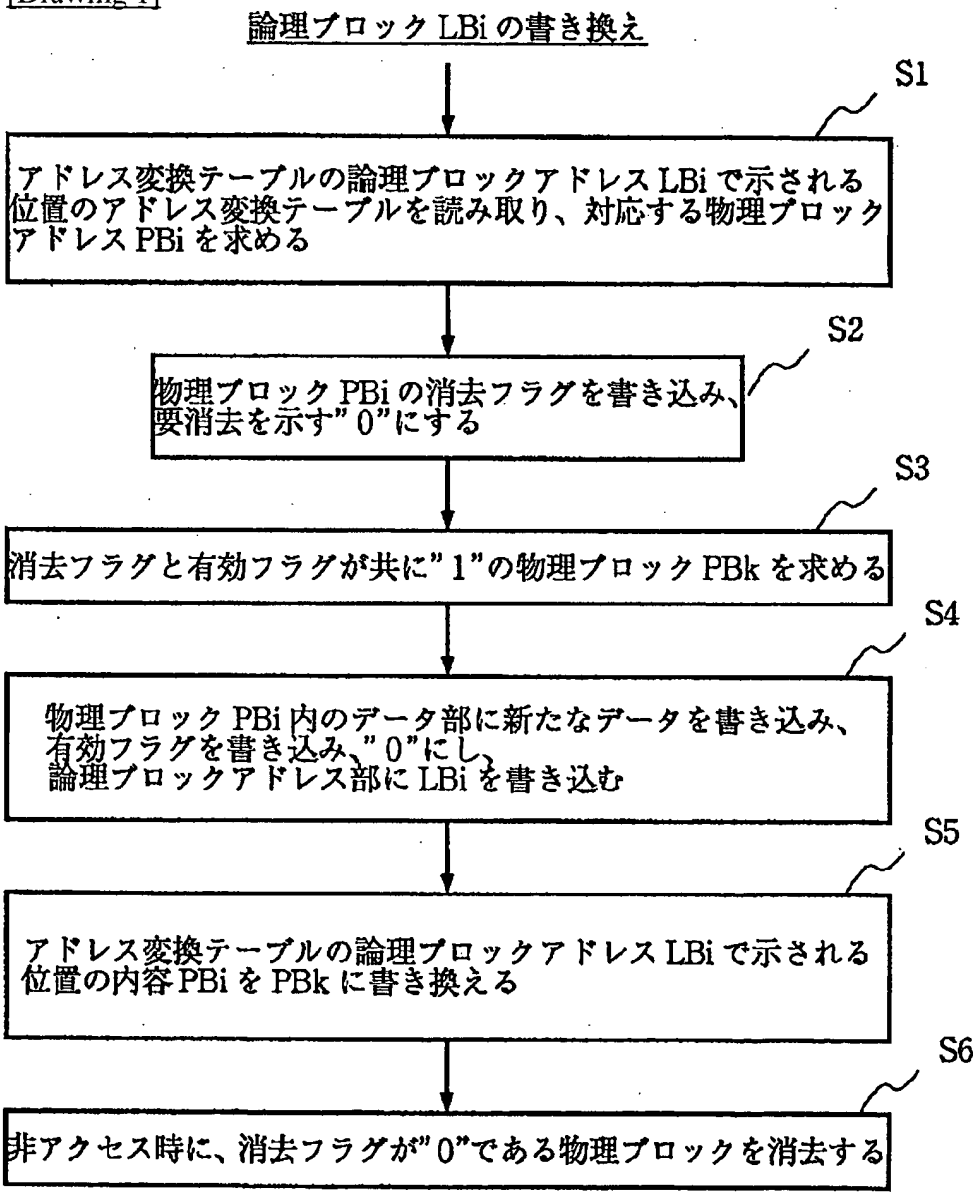
[Claim 1] The count of rewriting of the elimination flag field which consists of the sector of two or more memory capacity defined beforehand, and stores an elimination flag for every physical block of said block at least, the effective flag field which stores an effective flag, the logic block-address field which stores a logic block address, and said physical block It consists of two or more blocks which have the count field of rewriting to store, and the data area which stores data. In the non-volatile semiconductor memory which performs each elimination of the content of storing of said elimination flag, said effective flag, said logic block address, and said count of rewriting in the unit of said block, and performs read-out write-in actuation of said block of each in the unit of said sector The non-volatilized student semiconductor memory characterized by having the translation table changed into a physical block address from said logic block address at the time of read-out write-in actuation of said block.

[Claim 2] The count of rewriting of the elimination flag field which consists of the sector of two or more memory capacity defined beforehand, and stores an elimination flag for every physical block of said block at least, the effective flag field which stores an effective flag, the logic block-address field which stores a logic block address, and said physical block It consists of two or more blocks which have the count field of rewriting to store, and the data area which stores data. In the control approach of a non-volatile semiconductor memory of performing each elimination of the content of storing of said elimination flag, said effective flag, said logic block address, and said count of rewriting in the unit of said block, and performing read-out write-in actuation of said block of each in the unit of said sector It has the translation table changed into a physical block address from said logic block address at the time of read-out write-in actuation of said block. In case data are rewritten, the data specified by said logic block address It asks for the 1st physical block address corresponding to said logic block address from said address translation table. The elimination flag field of the 1st block specified by this 1st physical block address is written in important point elimination. It asks for the 2nd physical block address [finishing / elimination] an elimination flag indicates elimination needlessness to be and an effective flag indicates an invalid to be. The effective flag which is specified by this 2nd physical block address and which shows validity is written in the effective flag field of a block of said logic block address of the write-in above 2nd to the logic block-address field of a block of said data of the write-in above 2nd in the data area of the 2nd block. Said 2nd physical block address is written in the address specified by said logic block address of said address translation table. An elimination flag is important point elimination at the period when it is made to correspond to the storage condition after eliminating the invalid of the elimination needlessness of the elimination flag of said 1st block, and the effective flag of said 1st block at, and said non-volatile semiconductor memory is not accessed. An effective flag an invalid The control approach of the non-

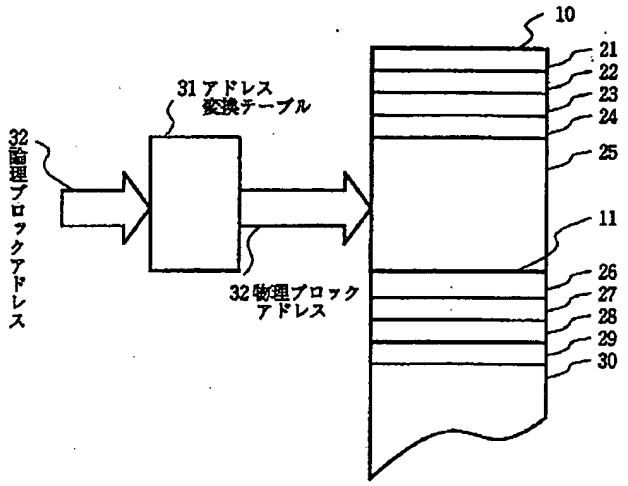
volatile semiconductor memory characterized by eliminating the shown block.
[Claim 3] The control approach of the non-volatile semiconductor memory according to claim 2 characterized by rewriting at the period when said non-volatile semiconductor memory is not accessed, and eliminating little block of a count.

DRAWINGS

[Drawing 1]

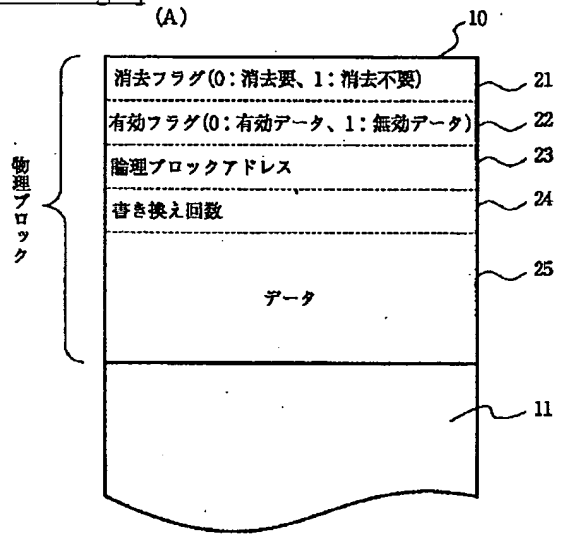


[Drawing 2]

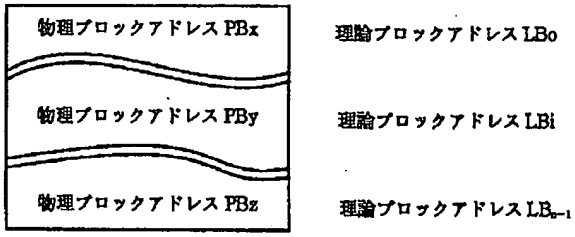

10
21
22
23
24
25
11
26
27
28
29
30
31 アドレス
変換テーブル
32 論理ブロックアドレス
32 物理ブロック
アドレス

[Drawing 3]

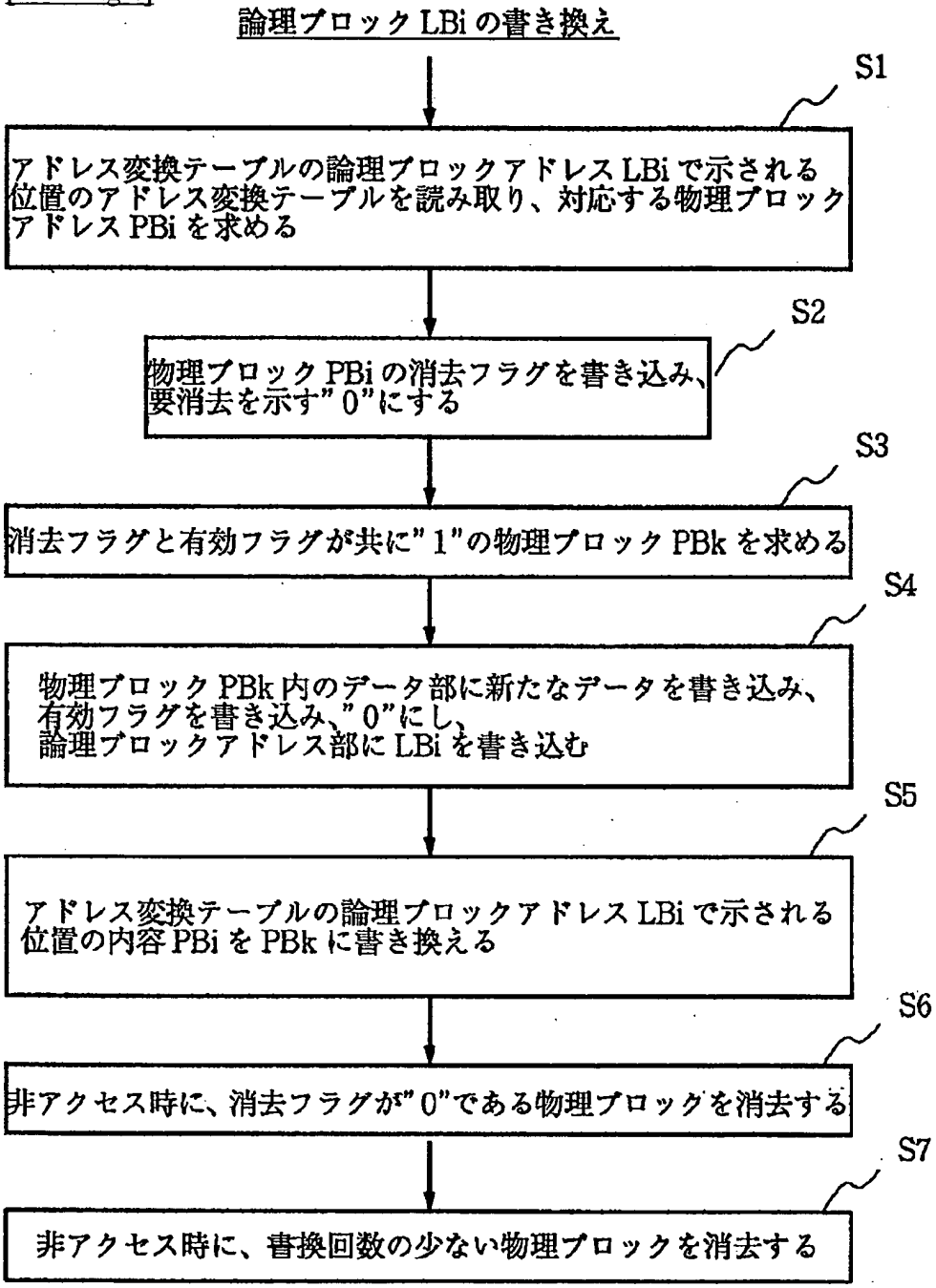
(A)


10
消去フラグ(0：消去要、1：消去不要)
有効フラグ(0：有効データ、1：無効データ)
論理ブロックアドレス
書き換え回数
データ
物理ブロック
21
22
23
24
25
11

(B)


物理ブロックアドレス PBx
物理ブロックアドレス PBy
物理ブロックアドレス PBz
理論ブロックアドレス LBo
理論ブロックアドレス LBi
理論ブロックアドレス LBn-1

[Drawing 4]



[Translation done.]